MEMSYS 2025

The International Symposium on Memory Systems ❖ 07.10.2025 - 09.10.2025, Washington DC

Important Dates

Abstract Deadline: 2 June, 2025

Submission: 9 June, 2025

Notification: 14 July, 2025

Camera-Ready: 11 August, 2025

Submission Formats

You may submit any length of an original document — anything from 1–16 pages is acceptable, for example:

1–2 page **Abstracts**
5–6 page **Position Papers**
10+ page **Research Papers**

Conference paper format, ACM 'sigconf' proceedings template, blind submission (no authors listed), up to 16 pages long

Organizers

Bruce Jacob (Naval Academy)
Abdel-Hameed Badawy (NMSU)
Atanu Barai (LANL)
Jonathan Beard (Google)
Vito Giovanni Castellana (PNNL)
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Memory-device manufacturing, memory-architecture design, and the use of memory technologies by application software all profoundly impact today's and tomorrow's computing systems, in terms of their performance, function, reliability, predictability, power dissipation, and cost. Existing memory technologies are seen as limiting in terms of power, capacity, and bandwidth. Emerging memory technologies offer the potential to overcome both technology- and design-related limitations to answer the requirements of many different applications. Our goal is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, to update each other on the latest state of the art, to exchange ideas, and to discuss future challenges. *Please visit **memsys.io** for more information.*

Areas of Interest

Previously unpublished papers containing significant novel ideas and technical results are solicited. Papers that focus on system, software, and architecture level concepts specifically memory-related, i.e. topics outside of traditional conference scopes, will be preferred over others (e.g., the desired focus is away from pipeline design, processor cache design, prefetching, data prediction, etc.). Symposium topics include, but are not limited to, the following:

- Memory-system design from both hardware and software perspectives
- Memory failure modes and mitigation strategies
- Memory and system safety and security issues
- Disaggregated Memory (e.g. CXL)
- Memory for embedded and autonomous systems (e.g., automotive)
- Operating system design for hybrid/nonvolatile memories
- Technologies including, DRAM, FLASH, NVM etc.
- Memory-centric programming models, languages, optimization
- Compute-in-memory and compute-near-memory technologies
- Data-movement issues and mitigation techniques
- Algorithmic & software memory-management techniques
- Emerging memory technologies, their controllers, and novel uses
- Interference at the memory level across datacenter applications
- In-memory databases and NoSQL stores
- Post-CMOS scaling efforts and memory technologies to support them, including cryogenic, neural, and heterogeneous memories
- Negative results, validation of results, invalidation of results

To reiterate, papers that focus on topics *outside* the scope of traditional architecture conferences will be preferred over others.

Submissions and Presentations

Our primary goal is to showcase interesting ideas that will spark conversation between disparate groups—to get applications people, operating systems people, system architecture people, interconnect people and circuits people to talk to each other. We accept extended abstracts, position papers, and/or full research papers, and each accepted submission is given a 20-minute presentation time slot.

We intend to publish all papers in the ACM Digital Library.

Venue

The conference will be in Melrose Georgetown Hotel in Washington DC