Critical Issues in Advanced ReRAM Development

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Abstract

For many years, Resistive RAM (ReRAM) technology has been pursued as a potentially high yield 3D memory. Recent improvements include the addition of diode-select devices that reduce sneak path leakages. These memory structures can be made using only back-end-of-the-line processing steps. ReRAM materials are fully compatible with backend processes and the resulting memories are planar, stackable units. No active devices are present in these stacks. These devices are highly suitable for new memory architectures, such as edge computing or compute-in-memory. We have developed interlayer interconnect architectures that minimize individual cell sizes, which we disclose in this paper. Persistent problems remain. These include poor device yield and poor cycle endurance. These issues can be traced to the basic mechanism of ReRAM operation: the formation (and destruction) of conducting filaments creating the set and reset states. The tips of these filaments develop exceptionally high electric fields due to field-line compression (lightning rod effect). The filament tips will undergo field-forming rearrangement, leading to arc-over and ultimate device failure. In this paper, we describe alternative methods of conduction bridge formation in which these high fields are not necessary for realizing the set/reset cycle. In conventional ReRAM devices, current flow during read and write is perpendicular to the chip surface. In the structures we propose, current flow is horizontal with respect to this surface. We refer to these devices as HReRAMs. Process flows and characterization results for these structures will be prescribed in this paper.