Extending the Life of Old Systems with More Memory

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ABSTRACT

Extending the lifetime of computing systems is definitely one of the ways to reduce CO_2. In this paper, we explore and suggest the options of extending memory in old systems by utilizing CXL technologies.

CCS CONCEPTS

• **Computer systems organization → Processors and memory architectures**; • **Hardware → Impact on the environment**.

KEYWORDS

CO_2, green computing, memory, reuse, CXL

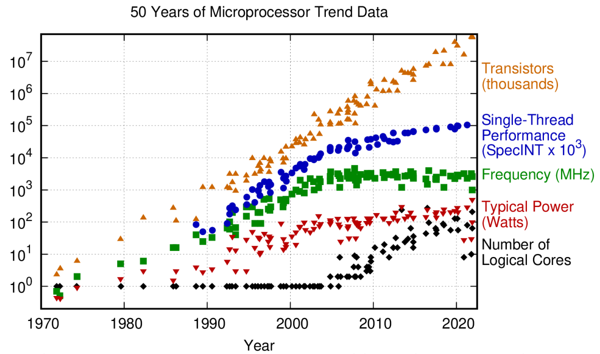
1 INTRODUCTION

As we approach the end of Dennard Scaling, the performance increases of single-thread processor performance have been slowed down. As Figure 1 shows, for the last decade (since 2010), typical power consumption and the frequency of the processor has plateaued.

However, modern workloads face a dual challenge. One challenge is that the size of the data to process is increasing, as shown in [17][15]. However, the attained results would not have been possible without the huge amounts of processed data. Importantly, the sizes of the graphs are increasing at a dizzying rate [8][1]. This growth in the amount of data is an enabler of new applications, but it is also a bottleneck in their progress because of exponentially growing demand for memory and the poor and slowing scaling properties of DRAM [22].

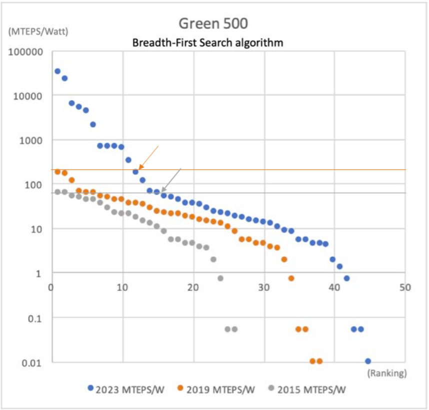
We have observed that the power efficiency of high performance computing systems has increased continuously despite the observation in Figure 1. Figure 2, the Green500 ranking based on the ratio of Millions of TeraFloatingPoint Operations Per Second (MTEPS) to Watt (MTEPS/Watt) is presented for three points in time: the current year (2023), as well as 4 and 8 years ago. Notably, it has been observed that the top 10 systems in 2019 maintain their dominance, remaining at the top 20% of the 2023 ranking. Similarly, the leading 2015 systems retain their importance, occupying the upper 40% of the 2023 ranking. This intriguing pattern signifies that even after a decade, the supercomputer systems that were at the forefront in earlier years continue to hold a position of median performance in 2023.

The other challenge is that the world is warming up, and this is in large part a result of Greenhouse Gas (GHG) emissions. This climate change leads to severe and devastating weather-related events [7]. To respond to this problem, we propose to leverage the potential to reuse technologies as part of the US Environmental Protection Agency's (EPA) "reduce, reuse, and recycle" mantra and strategy [3, 13]. We propose to increase the memory in the high-performance computing systems to extend the life time of computing systems. In particular, we explore the option of using the recent CXL technology [21].



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2021 by K. Rupp

Figure 1: 50 Years of Microprocessor Trend Data. Image Source: [20]. This chart is provided under the permissive 'Creative Commons Attribution 4.0 International Public License.'



Green500 website data available from 2013 - 2023 (https://graph500.org)

Figure 2: Green500 $\frac{MTEPS}{Watt}$ ranking.

2 BACKGROUND OF CXL TECHNOLOGY

CXL is a high-speed CPU interconnect technology standard developed and maintained by the Compute Express Link consortium. We provide the following background as a brief summary of the more in-depth material found in [2, 9, 19, 21].

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The notable characteristic of CXL is that its Flex Bus leverages PCIe PHY for its physical layer. What this means is that any computer or device that supports compatible PCIe versions can support CXL.

CXL structure: The CXL Link layer is responsible for CRC checks and flow control through a credit system. The CXL transaction layer is responsible for Flit packing and unpacking and for processing and storing the transactions in queues. CXL is comprised of three sub-protocols, namely CXL.io, CXL.cache, and CXL.memory, which have the function of supporting I/O, cache coherency, and memory semantics, respectively.

CXL versions: CXL 1.0 (released March 2019) and CXL 1.1 (released September 2019) introduced the suit of sub-protocols that constitute the CXL standard. CXL maintains coherency in memory spaces between the CPU and any attached device. CXL 1.1 defined three types of devices based on differing use cases: Type 1, Type 2, and Type 3. Type 1 devices leverage CXL.cache and are caching devices or accelerators such as smart NICs. Type 2 devices are accelerators with memory such as GPGPUs with local memory that is mapped to a cacheable system memory and leverage CXL.cache and CXL.memory. Type 3 devices leverage CXL.memory and have the purpose of serving as memory buffers by expanding memory bandwidth or capacity and can be used to connect together different memory types. In addition, all three types make use of CXL.io. CXL 2.0 (released November 2020) enhanced the protocol by introducing support for, among the most relevant, switch capability and memory pooling. CXL 3.0 (released Q3 2022) doubles the bandwidth and introduces multiple level switching, it also enables non-tree topologies and peer-to-peer communication, and it introduces Global Fabric Attached Memory (GFAM) devices which disaggregates the memory from the processing unit and implements a memory pool.

3 MACHINE EXTENSIONS WITH CXL MEMORY

We begin the following analysis assuming that the trivial solution of simply adding more memory in the high-performance computing systems without any further change is not an option as we assume that the current motherboard is maxed out on available memory slots and capacity. Hence, we try to answer the following simple question: *Can we increase the memory of old systems using CXL technologies, since CXL is based on PCIe?*

3.1 About PCIe Versions

Unfortunately, the earlier versions of CXL require at least PCIe 5.0 [2], which debuted in 2019. It is important to note that previous versions of CXL, namely CXL 1.1 and CXL 2.0 are compatible with 32 GT/s PCIe 5.0 and CXL 3.0 is compatible with 64 GT/s PCIe 6.0. Notably, all CXL versions are backward compatible. AMD Epyc (2022) and Intel Xeon (2023) servers started supporting PCIe 5.0 starting with their 4th generations. AMD Epyc supported PCIe 4.0 starting with its 2nd (2019) and 3rd generation, and Intel Xeon supported PCIe 4.0 starting with its 3rd Generation (2020) [4, 14]. Unfortunately, PCIe supports are also part of CPU specification as I/O design is a part of the protocols. Consequently, to enable the utilization of older systems with CXL, it becomes necessary to replace both the microprocessor and the chipset. This implies that merely swapping out motherboards for the purpose of expanding memory is not a feasible solution for upgrading legacy systems. An alternative would be to be able to use PCIe 4.0 systems with CXL. The downside of this would be that PCIe 4.0 only has half as much bandwidth as PCIe 5.0, which means that the memory bandwidth with CXL would be half as well. However, CXL with PCIe 5.0 is expected to provide up to 64 GB/s in each direction over a 16-lane link and the half of that is 32 GB/s in each direction over a 16-lane link. Compared to the bandwidth of SSD (300-600 MB/s), the performance with CXL with PCIe 4.0 would still provide higher performance than using storage as an extension of memory systems.

3.2 Adding Memory

There are two basic ways in which memory can be expanded to a system by leveraging CXL technologies. The first option explored is to add CXL Type 3 memory expansion modules such as [23]. This option enables leveraging CXL 2.0 to introduce memory modules in the form of add in cards. The second option explored is to leverage CXL Memory Pooling by using a memory pool controller such as [5]. While the original intent of memory pooling is to leverage memory from a variety of different sources from more than one system in order to avoid over-provisioning memory that can lead to memory stranding [6, 16] and to add to overall memory, we look at memory pooling as a means to compensate for older systems that may be reused [3, 13] that may only need more memory in order to perform at an acceptable level.

4 RELATED WORK

Research on the sustainability of computing systems has been gaining prominence recently, with researchers studying overall environmental sustainability as well as the specific aspects of sustainable computing [10–13, 18]. More directly related to our current research, Junkyard Computing [24] proposes to reuse mobile phones for processing. We propose to use old servers with added memory. [6] carries out an analysis of CXL pooling on Azure cloud and compares and explores CXL memory pool deployment strategies. Further, and more directly relevant to our paper, it suggests that economical costs may be reduced by reusing DDR4 from retired servers.

5 CONCLUSIONS

Based on the analysis provided, it is evident that CXL technology presents a promising opportunity to augment the memory capacity of current systems. However, it is crucial to note that compatibility with existing machines is highly dependent on the specific PCIe version employed.

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